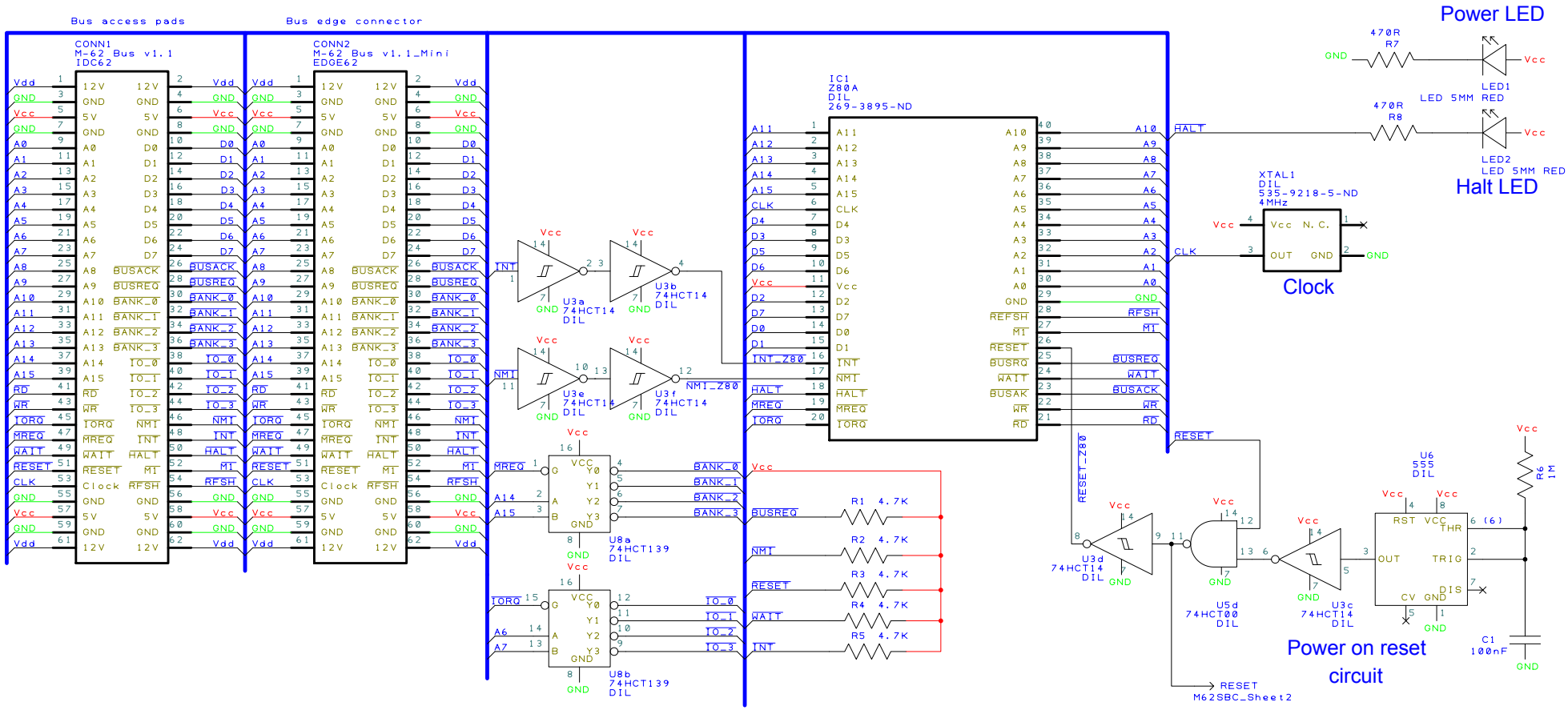
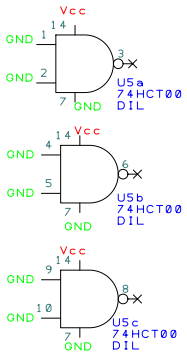
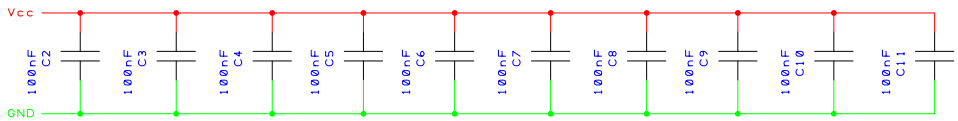
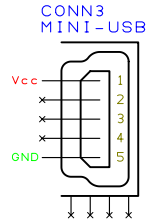


Spare gates



Decoupling capacitors

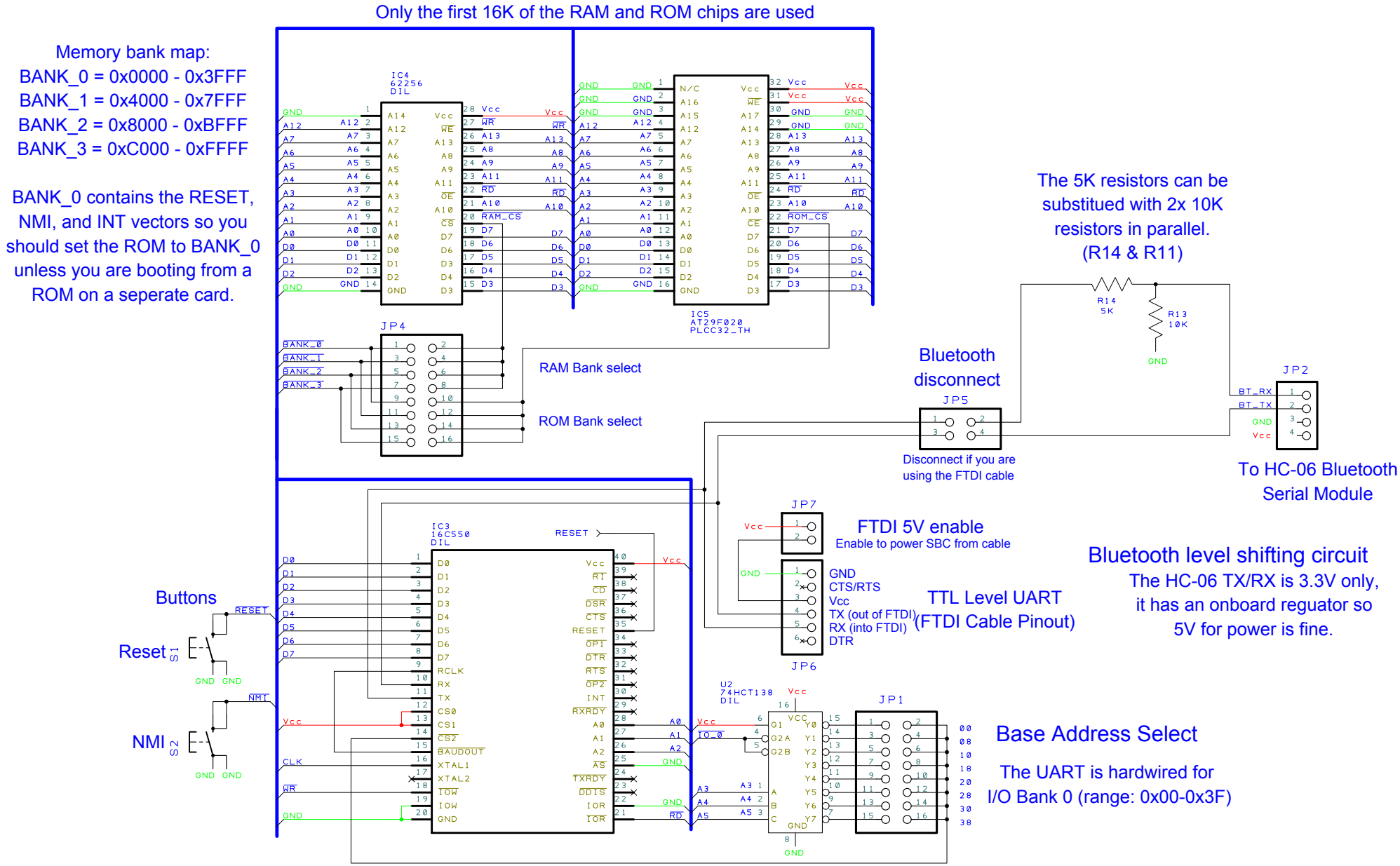




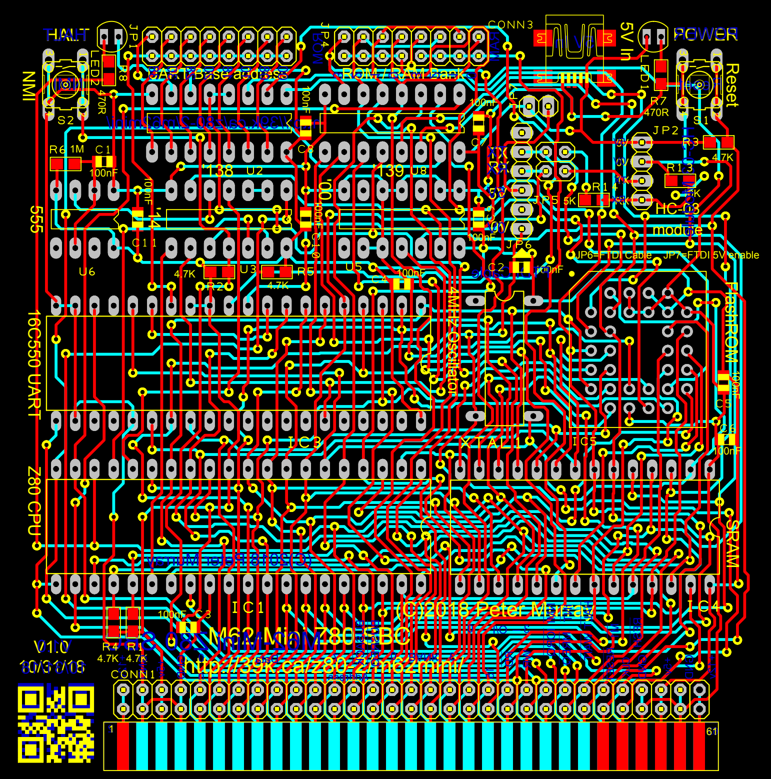
5V power only

for development when not in the M62 Bus backplane

Murray Electronics (C)2018 Peter Murray	Design: Z80 CPU / Bank decode / M62 interface	Designer: PM	Version: 1.0	Date:	Sheet: 1 / 2



Murray Electronics (C)2018 Peter Murray	Design: ROM / RAM / UART	Designer: PM	Version: 1.0	Date:	Sheet: 2 / 2



HALT
POWER
NMI
Reset
5V In
CONN3
UART Base address
ROM / RAM Bank
'138
U2
'139
U8
555
U6
16C550 UART
Z80 CPU
4MHz Oscillator
XTAL1
FlashROM
SRAM
IC1
IC3
IC4
IC5
HC-05 module
JP6=FTDI Cable
JP7=FTDI 5V enable
(C)2018 Peter Murray
M62 Mini Z80 SBC
http://39k.ca/z80-2/m62mini/
V1.0
CONN1